

DATA SHEET

74LVT2952

**3.3V LVT octal registered transceiver
(3-State)**

Product specification
Supersedes data of 1994 Sep 27
IC23 Data Handbook

1998 Feb 19

3.3V Octal registered transceiver (3-State)

74LVT2952

FEATURES

- 8-bit registered transceiver
- Independent registers for A and B buses
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Power-up reset
- Power-up 3-State
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT2952 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device combines low static and dynamic power dissipation with high speed and high output drive.

The 74LVT2952 device is an 8-bit registered transceiver. Two 8-bit back-to-back registers store data flowing in both directions between two bidirectional buses.

Data applied to the inputs is entered and stored on the rising edge of the Clock (CPXX) provided that the Clock Enable (\overline{CEXX}) is Low. The data is then present at the 3-State output buffers, but is only accessible when the Output Enable (\overline{OEXX}) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

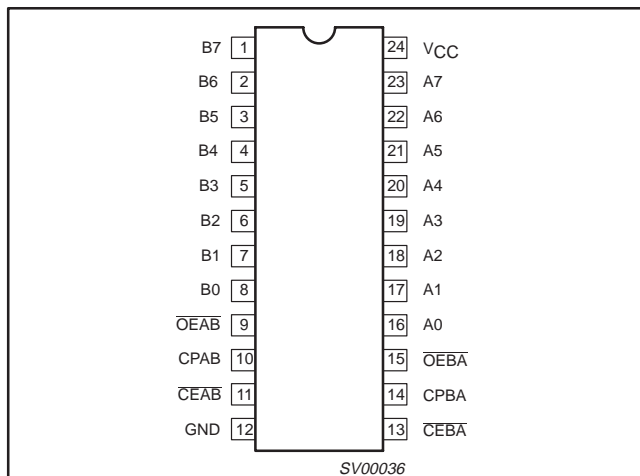
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPBA to An or CPAB to Bn	$C_L = 50\text{pF}; V_{CC} = 3.3\text{V}$	3.1 3.8	ns
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or 3.0V	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O} = 0\text{V}$ or 3.0V	8	pF
I_{CCZ}	Total supply current	Outputs disabled; $V_{CC} = 3.6\text{V}$	0.13	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic SOL	-40°C to $+85^{\circ}\text{C}$	74LVT2952 D	74LVT2952 D	SOT137-1
24-Pin Plastic SSOP Type II	-40°C to $+85^{\circ}\text{C}$	74LVT2952 DB	74LVT2952 DB	SOT340-1
24-Pin Plastic TSSOP Type I	-40°C to $+85^{\circ}\text{C}$	74LVT2952 PW	7LVT2952PW DH	SOT355-1

PIN CONFIGURATION



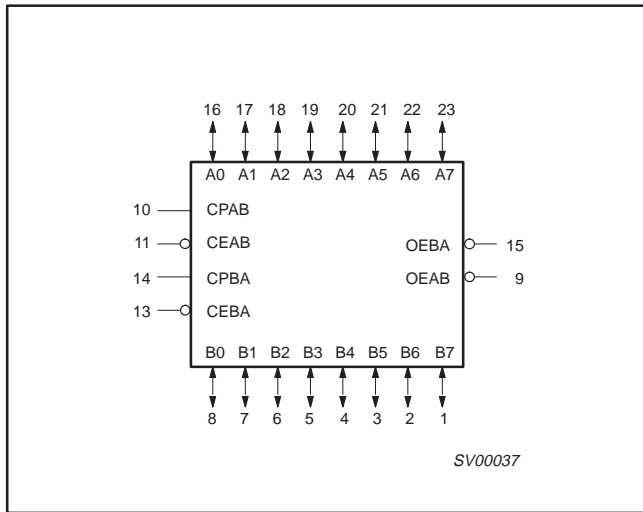
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
10, 14	CPAB / CPBA	Clock input A to B / Clock input B to A
11, 13	$\overline{CEAB} / \overline{CEBA}$	Clock enable input A to B / Clock enable input B to A
16, 17, 18, 19, 20, 21, 22, 23	A0 – A7	Data inputs/outputs (A side)
8, 7, 6, 5, 4, 3, 2, 1	B0 – B7	Data outputs/outputs (B side)
9, 15	$\overline{OEAB} / \overline{OEBA}$	Output enable inputs
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

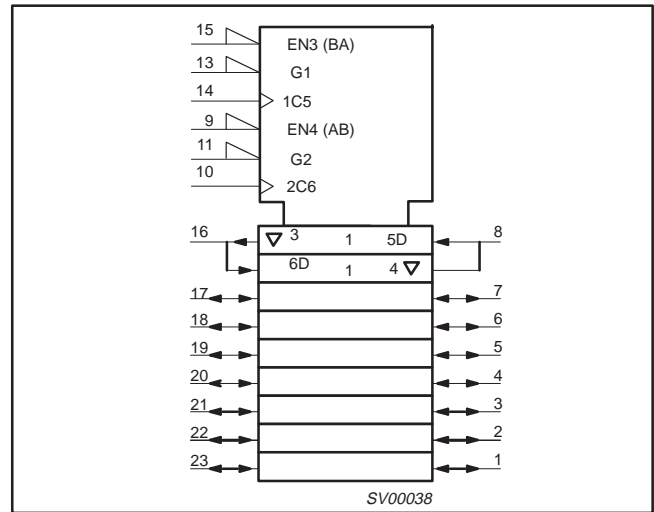
3.3V Octal registered transceiver (3-State)

74LVT2952

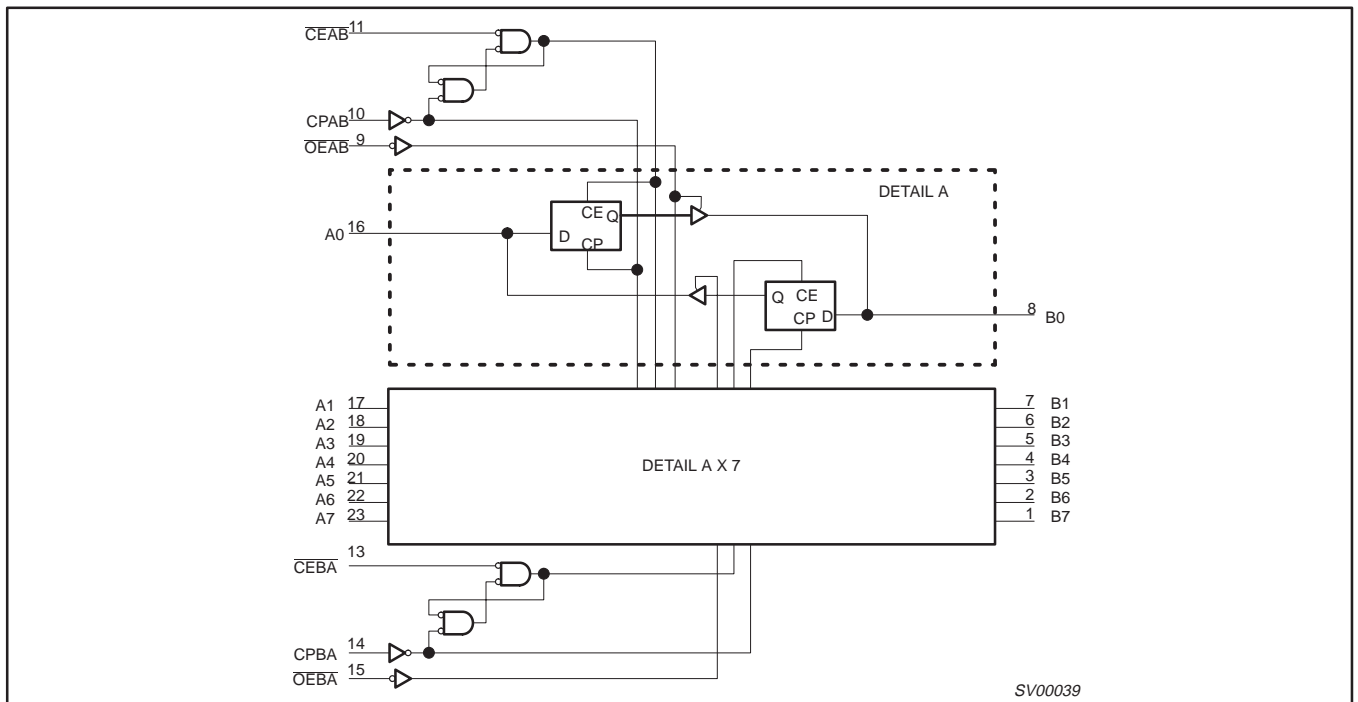
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE for Register An or Bn

INPUTS			INTERNAL Q	OPERATING MODE
An or Bn	CPXX	CEXX		
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	

H = High voltage level
 L = Low voltage level
 ↑ = Low-to-High transition
 X = Don't care
 XX = AB or BA
 NC = No change

FUNCTION TABLE for Output Enable

INPUTS	INTERNAL Q	An or Bn OUTPUTS	OPERATING MODE
OEXX			
H	X	Z	Disable outputs
L	L	L	Enable outputs
L	H	H	

H = High voltage level
 L = Low voltage level
 X = Don't care
 XX = AB or BA
 Z = High impedance "off" state

3.3V Octal registered transceiver (3-State)

74LVT2952

ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +4.6	V
I _{IK}	DC input diode current	V _I < 0	-50	mA
V _I	DC input voltage ³		-0.5 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	-50	mA
V _{OUT}	DC output voltage ³	Output in Off or High state	-0.5 to +7.0	V
I _{OUT}	DC output current	Output in High state	-64	mA
		Output in Low state	128	
T _{stg}	Storage temperature range		-65 to 150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V _{CC}	DC supply voltage	2.7	3.6	V
V _I	Input voltage	0	5.5	V
V _{IH}	High-level input voltage	2.0		V
V _{IL}	Low-level Input voltage		0.8	V
I _{OH}	High-level output current		-32	mA
I _{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%, f ≥ 1kHz		64	
Δt/Δv	Input transition rise or fall rate; Outputs enabled		10	ns/V
T _{amb}	Operating free-air temperature range	-40	+85	°C

3.3V Octal registered transceiver (3-State)

74LVT2952

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 2.7V; I _{IK} = -18mA		-0.9	-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 2.7 to 3.6V; I _{OH} = -100μA	V _{CC} -0.2	V _{CC} -0.1		V
		V _{CC} = 2.7V; I _{OH} = -8mA	2.4	2.5		
		V _{CC} = 3.0V; I _{OH} = -32mA	2.0	2.2		
V _{OL}	Low-level output voltage	V _{CC} = 2.7V; I _{OL} = 100μA		0.1	0.2	V
		V _{CC} = 2.7V; I _{OL} = 24mA		0.3	0.5	
		V _{CC} = 3.0V; I _{OL} = 16mA		0.25	0.4	
		V _{CC} = 3.0V; I _{OL} = 32mA		0.3	0.5	
		V _{CC} = 3.0V; I _{OL} = 64mA		0.4	0.55	
V _{RST}	Power-up output low voltage ⁵	V _{CC} = 3.6V; I _O = 1mA; V _I = GND or V _{CC}		0.13	0.55	V
I _I	Input leakage current	V _{CC} = 3.6V; V _I = V _{CC} or GND	Control pins	±0.1	±1.0	μA
		V _{CC} = 0 or 3.6V; V _I = 5.5V		1	10	
		V _{CC} = 3.6V; V _I = 5.5V	I/O Data pins ⁴	1	20	
		V _{CC} = 3.6V; V _I = V _{CC}		0.1	1.0	
		V _{CC} = 3.6V; V _I = 0		-1	-5.0	
I _{OFF}	Output off current	V _{CC} = 0V; V _I or V _O = 0 to 4.5V		1	±100	μA
I _{HOLD}	Bus Hold current A inputs ⁶	V _{CC} = 3V; V _I = 0.8V	75	150		μA
		V _{CC} = 3V; V _I = 2.0V	-75	-150		
		V _{CC} = 0V to 3.6V; V _{CC} = 3.6V	±500			
I _{EX}	Current into an output in the High state when V _O > V _{CC}	V _O = 5.5V; V _{CC} = 3.0V		60	125	μA
I _{PU/PD}	Power up/down 3-State output current ³	V _{CC} ≤ 1.2V; V _O = 0.5V to V _{CC} ; V _I = GND or V _{CC} ; OE/OE = Don't care		±1	±100	μA
I _{CCH}	Quiescent supply current	V _{CC} = 3.6V; Outputs High, V _I = GND or V _{CC} , I _O = 0		0.13	0.19	mA
I _{CCL}		V _{CC} = 3.6V; Outputs Low, V _I = GND or V _{CC} , I _O = 0		3	12	
I _{CCZ}		V _{CC} = 3.6V; Outputs Disabled; V _I = GND or V _{CC} , I _O = 0		0.13	0.19	
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 3V to 3.6V; One input at V _{CC} - 0.6V, Other inputs at V _{CC} or GND		0.1	0.2	mA

NOTES:

- All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
- This is the increase in supply current for each input at V_{CC} = 0.6V.
- This parameter is valid for any V_{CC} between 0V and 1.3V with a transition time of up to 10msec. From V_{CC} = 1.3V to V_{CC} = 3.3V ± 0.3V a transition time of 100μsec is permitted. This parameter is valid for T_{amb} = 25°C only.
- Unused pins at V_{CC} or GND.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

3.3V Octal registered transceiver (3-State)

74LVT2952

AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$, $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$	
			MIN	TYP ¹	MAX	MAX	
f_{MAX}	Maximum clock frequency	1	150	200			MHz
t_{PLH} t_{PHL}	Propagation delay CPBA to An, CPAB to Bn	1	1.3 1.8	3.1 3.8	6.1 6.0	7.1 6.9	ns
t_{PZH} t_{PZL}	Output enable time $\overline{\text{OEBA}}$ to An, $\overline{\text{OEAB}}$ to Bn	3 4	1.0 1.2	3.4 3.6	5.6 6.5	6.7 8.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{\text{OEBA}}$ to An, $\overline{\text{OEAB}}$ to Bn	3 4	1.0 1.6	3.7 3.4	6.3 5.1	6.9 5.3	ns

NOTE:

1. All typical values are at $V_{CC} = 3.3V$ and $T_{\text{amb}} = 25^\circ\text{C}$.

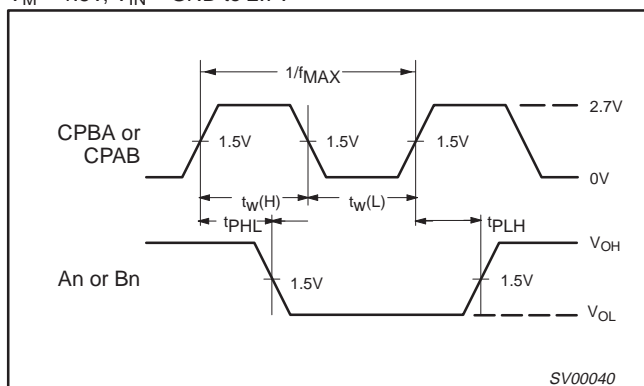
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$, $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

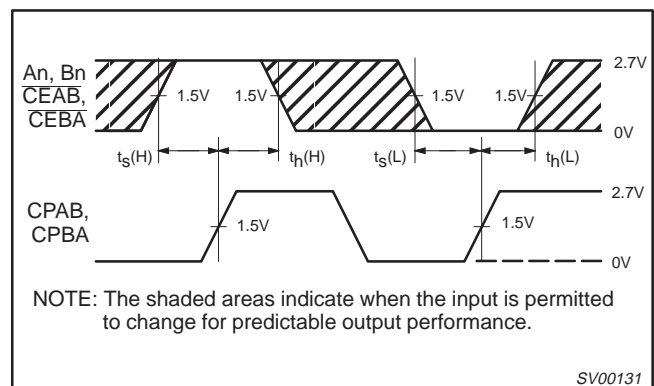
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$	
			MIN	TYP ¹	MIN	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time An to CPAB or Bn to CPBA	2	2.5 2.5	1 1	2.8 3.0	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time An to CPAB or Bn to CPBA	2	1.5 2.5	-0.5 -0.5	0.7 2.6	ns
$t_s(\text{H})$ $t_s(\text{L})$	Setup time $\overline{\text{CEAB}}$ to CPAB or $\overline{\text{CEBA}}$ to CPBA	2	0.9 2.4	0.3 -0.3	0.8 2.7	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time $\overline{\text{CEAB}}$ to CPAB or $\overline{\text{CEBA}}$ to CPBA	2	1.5 2.5	0.3 0	0.7 2.6	ns
$t_w(\text{H})$ $t_w(\text{L})$	CPAB or CPBA pulse width High or Low	1	3.3 3.3	1 1	3.3 3.3	ns

AC WAVEFORMS

$V_M = 1.5V$, $V_{\text{IN}} = \text{GND}$ to $2.7V$



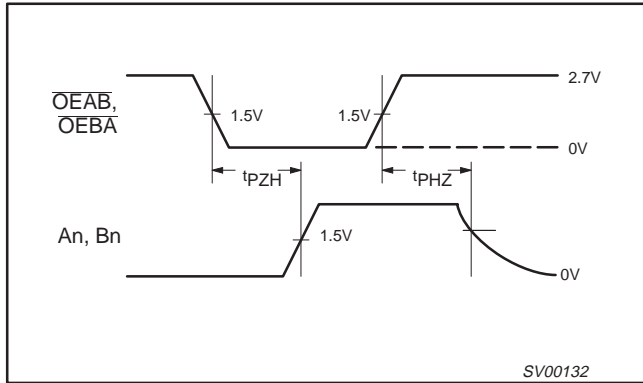
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



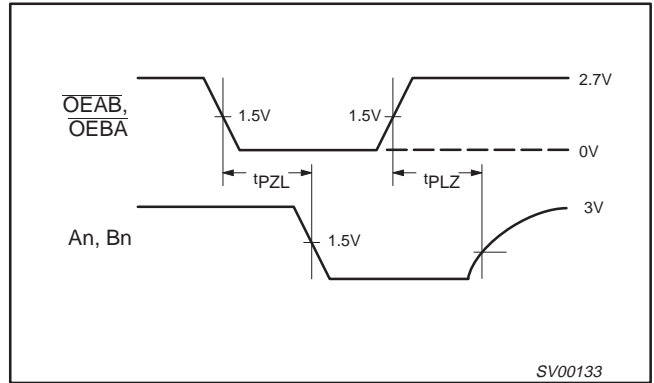
Waveform 2. Data Setup and Hold Times

3.3V Octal registered transceiver (3-State)

74LVT2952



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS

Test Circuit for 3-State Outputs

$V_M = 1.5V$
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SV00092

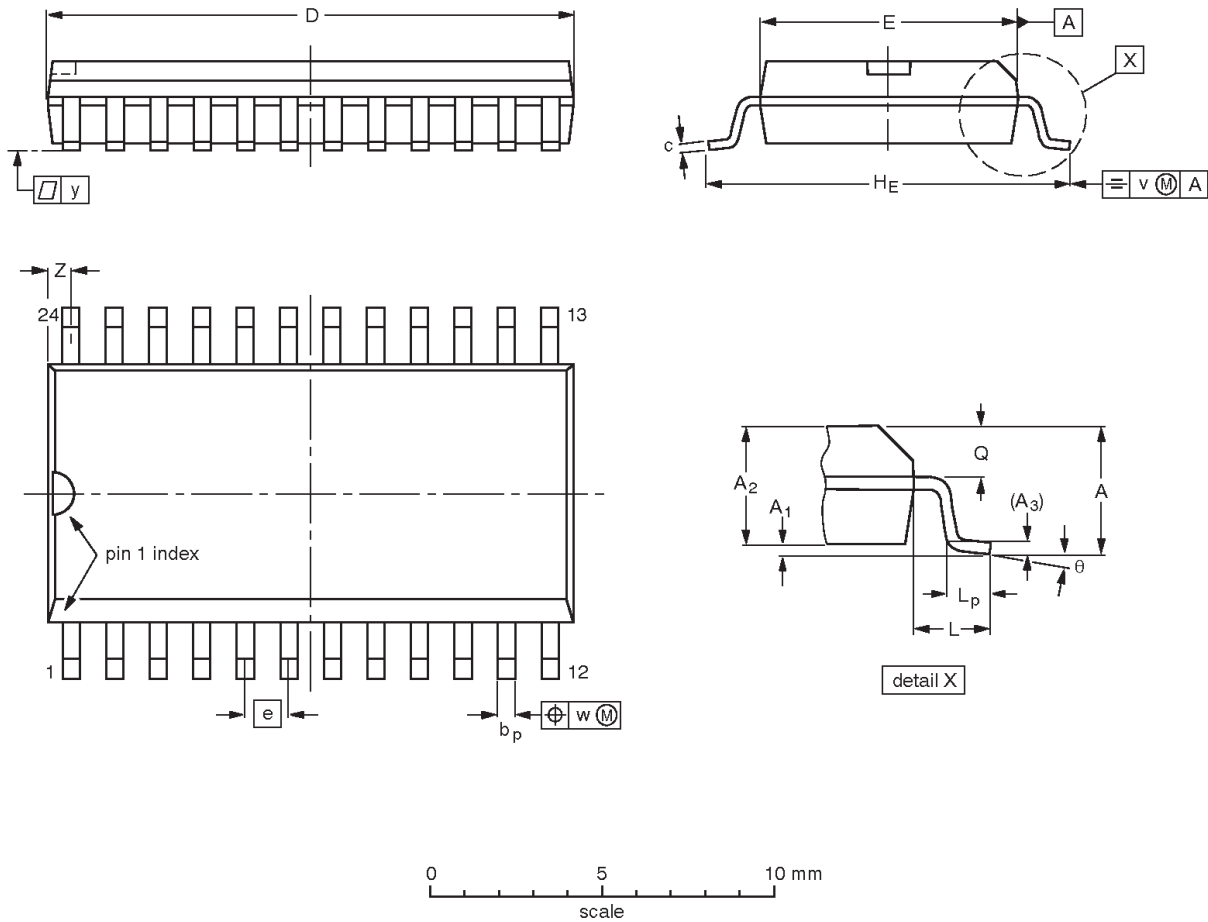
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_w	t_R	t_F
74LVT	2.7V	$\leq 10MHz$	500ns	$\leq 2.5ns$	$\leq 2.5ns$

3.3V LVT octal registered transceiver (3-State)

74LVT2952

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

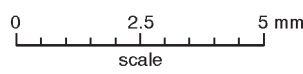
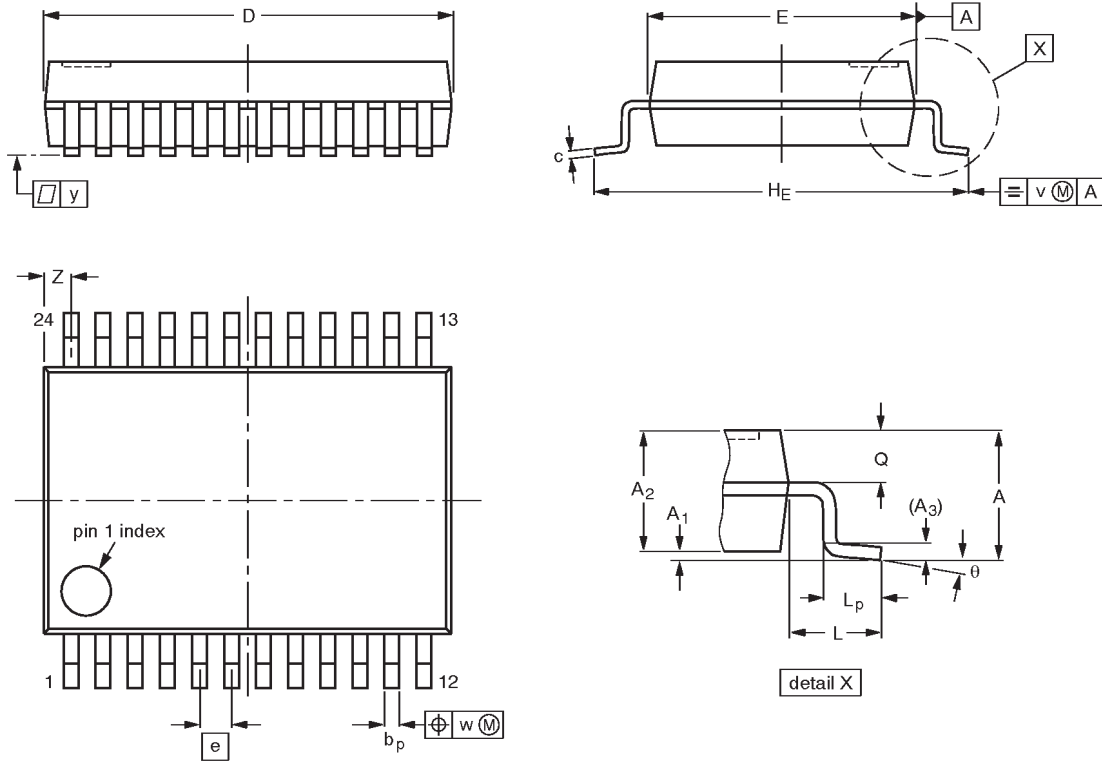
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				95-01-24 97-05-22

3.3V LVT octal registered transceiver (3-State)

74LVT2952

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

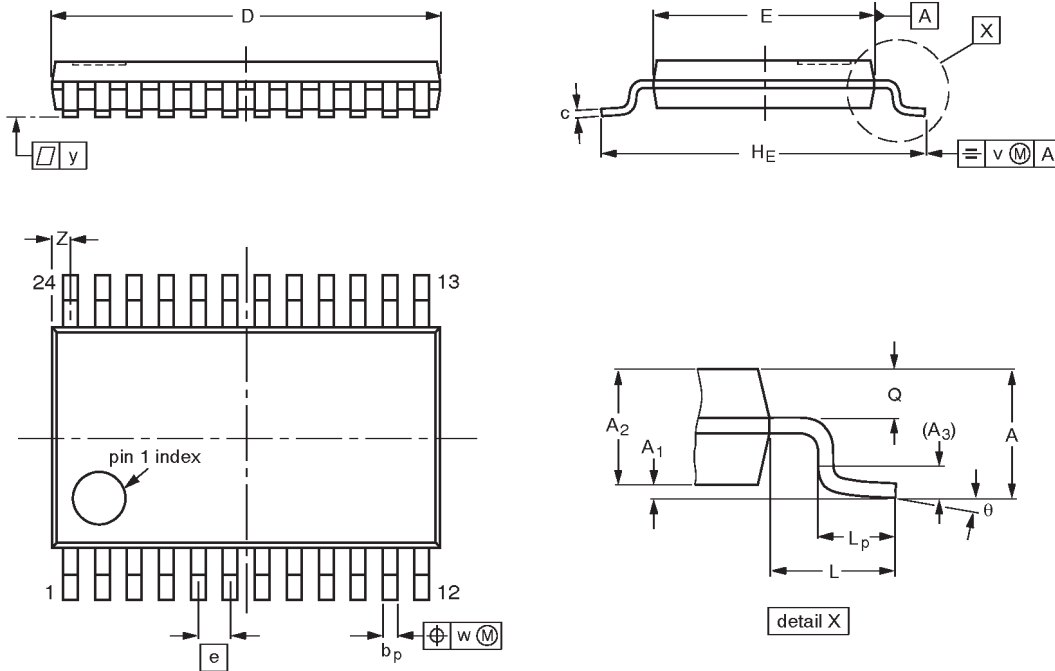
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				93-09-08- 95-02-04

3.3V LVT octal registered transceiver (3-State)

74LVT2952

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				-93-06-16 95-02-04

3.3V LVT octal registered transceiver (3-State)

74LVT2952

NOTES

3.3V LVT octal registered transceiver (3-State)

74LVT2952

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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